UNITED STATES PATENT AND TRADEMARK OFFICE

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER
SONG, JASMINE

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2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

Detailed Action

Specification

The lengthy specification has not been checked to the extent necessary to

determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the

specification.

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found

to conform to the requirements prescribed in 37 C.F.R. 1.63.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly
claiming the subject matter which the applicant regards as his invention.

Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

The claim language "substantially" in claims 1, 14, 25, 28 is not clear or distinct.

This language is not defined in either the actual claim language or the specification. It is

not possible from either the specification or the claims to determine the scope of this

language or to determine the metes and bounds of the claim. Therefore, properly

rejected as indefinite under 35 U.S.C. 112, second paragraph.

In claim 1, 14, 25 and 28, applicant claims "perform **one or more** external

memory accesses, **the external memory accesses** having…; Examiner can interpret

this limitation as "perform one external memory access", therefore, it conflicts with the

limitation "the external memory accesses".

Claim 30 recites the limitation "the microengines" in line 1. There is insufficient

antecedent basis for this limitation in the claim.

all dependent claims are also rejected since they are depended on the rejected

independent claims

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
conditions and requirements of this title.

the claimed invention is directed to non-statutory subject matter. Claims 14-24

are not limited to tangible embodiments. In view of Applicant's disclosure, section 0027

and section 0075, the medium is not limited to tangible embodiments, instead being

defined as including both tangible embodiments (section 0027, lines 2-4) and intangible

embodiments (section 0027, lines 5-6; e.g., carrier wave, infrared signals, digital

signals, etc.). As such, the claim is not limited to statutory subject matter and is

therefore non-statutory. To overcome 101 rejection, the claims need to be amended to

include only the physical storage computer media and not a transmission media or other

intangible or non-functional media.

Claim Objections

Claims 26, 27, 29 are objected to because of the following informalities:

In claim 26, line 1, delete one "comprises".

In claim 27, "The data processing system of claim 26" should be changed to –

The processor claim 26--.

In claim 29, "The data processing system of claim 27" should be changed to –

The data processing system of claim 28--.

In claim 27, line 1, "the LM" should be changed to -- the local memory--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 7, 14-16 and 25-30 are rejected under 35 U.S.C. 102(e) as being

anticipated by Hammarlund e tal., US 7,085,889 B2

Regarding claims 1 and 14, Hammarlund teaches a method, comprising:

identifying a candidate representing a plurality of instructions of a plurality of

threads that perform one or more external memory accesses (Fig.3, it is taught as load

instructions LD0 and LD1 executed by the thread 0 and Thread 1), the external memory

accesses having a substantially identical base address (Fig.3, load instructions LD0 and

LD1 have identical base address); and inserting at least one of directives and

instructions into an instruction stream corresponding to the identified candidate (it is

taught as assign a context identifier to the instruction of the thread) to maintain contents

of at least one of a content addressable memory (CAM) and local memory (LM) of a

processor (col.3, lines 38-52) and to modify at least one of the external memory access

to access at least one of the CAM and LM of the processor without having to perform

the respective external memory access (col.5, lines 24-54).

Regarding claims 2 and 15, Hammarlund teaches further comprising: partitioning

the plurality of instructions of the external memory accesses into one or more sets of

potential candidates based on dependency relationships of the instructions (col.5, lines

17-33 and col.6, lines 9-31); and selecting one of the potential candidate sets as the

candidate, instructions of the candidate satisfying a predetermined dependency

relationship (col.5, lines 20-24).

Regarding claims 3 and 16, Hammarlund teaches further comprising converting

addresses of each external memory accesses into a form having a base address and

an offset (Fig.3 and col.2, lines 1-6).

Regarding claim 4, Hammarlund teaches the base address is a non-constant part

and the offset is a constant part of the converted address (col.2, lines 1-6).

Regarding claim 7, Hammarlund teaches the identifying the candidate further

comprises: performing a copy-forward transformation on addresses of each of the

external memory accesses; and performing at least one of a global value numbering

operation and a constant folding operation for each thread (col.6, lines 20-55).

Regarding claim 25, Hammarlund teaches a processor, comprising:

a plurality of microengines having a content addressable memory (CAM) and a

local memory respectively to perform a plurality of threads substantially concurrently

(Fig.3), each of the plurality of threads including one or more instructions performing at

least one external memory access (Fig.3, it is taught as load instructions LD0 and LD1

executed by the thread 0 and Thread 1) based on a base address that is substantially

identical (Fig.3, load instructions LD0 and LD1 have identical base address), wherein

the base address is examined in the CAM to determine whether the CAM includes an

entry containing the base address (col.3, lines 26-52), and wherein an entry of the local

memory corresponding to the entry of the CAM is accessed without having to accessing

the external memory, if the CAM includes the entry containing the base address (col.5,

lines 24-54).

Regarding claim 26, Hammarlund teaches the CAM of the microengines

comprises a least recently used (LRU) logic to allocate an LRU entry of the CAM linking

with an entry of the local memory, wherein the allocated LRU entry is used to cache the

external memory access for subsequent accesses to an identical location of the external

memory (col.6, lines 56-67, cache line replacement policies are well known in the art, a

least recently used replacement policy can be used in the Hammarlund to determine

which cache line will be used to store data).

Regarding claim 27, Hammarlund teaches the LM comprises an indexing logic to

provide an index pointing to an entry of the LM based on a reference supplied by the

LRU logic (Hammarlund mentioned index cache lines with a portion of a linear address

called a tag in co.2, lines 58-61).

Regarding claim 28, Hammarlund teaches a data processing system, comprising:

a processor (Fig.2 and 3 and col.1, lines 47 and 65);

a memory coupled to the processor; and a program instruction, when executed

from the memory (Fig.2 and 3), causes the processor to identifying a candidate

representing a plurality of instructions of a plurality of threads that perform one or more

external memory accesses (Fig.3, it is taught as load instructions LD0 and LD1

executed by the thread 0 and Thread 1), the external memory accesses having a

substantially identical base address (Fig.3, load instructions LD0 and LD1 have identical

base address); and inserting at least one of directives and instructions into an

instruction stream corresponding to the identified candidate (it is taught as assign a

context identifier to the instruction of the thread) to maintain contents of at least one of a

content addressable memory (CAM) and local memory (LM) of a processor (col.3, lines

38-52) and to modify at least one of the external memory access to access at least one

of the CAM and LM of the processor without having to perform the respective external

memory access (col.5, lines 24-54).

Regarding claim 29, Hammarlund teaches the plurality of threads is executed by a

plurality of microengines of the executing processor respectively, and wherein each of

the microengines of the executing processor includes a CAM and a LM (Fig.3).

Regarding claim 30, Hammarlund teaches the CAM of the microengines

comprises a least recently used (LRU) logic to allocate an LRU entry of the CAM to

cache a current external memory access for subsequent identical external memory,

access (col.6, lines 56-67, cache line replacement policies are well known in the art, a

least recently used replacement policy can be used in the Hammarlund to determine

which cache line will be used to store data), if the CAM does not contain the base

address of the current external memory access, and wherein the LM comprises an

indexing logic to provide an index pointing to an entry of the LM based on a reference

supplied by the LRU logic (Hammarlund mentioned index cache lines with a portion of a

linear address called a tag in co.2, lines 58-61).

Allowable Subject Matter

Claims 5-6, 8-13, 17-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jasmine Song/

Examiner, Art Unit 2188